TEXAS INSTRUMENTS

ADS7861/8361 EVM

User's Guide

October 2002

Data Acquisition Products

SLAU094

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3.3 Vdc to 5 Vdc and the output voltage range of 0 Vdc to 5 Vdc.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the ADS7861/8361 EVM – 12-/16-bit dual, 500-KSPS, 2+2 channel, serial analog-to-digital converter evaluation module. A complete circuit description as well as a schematic diagram and bill of materials are included.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 – EVM Overview
- Chapter 2 – Analog Interface
- Chapter 3 – Digital Interface
- Chapter 4 – Power Supplies
- Chapter 5 – EVM Operation
- Chapter 6 – Bill of Materials and EVM Schematic

Related Documentation From Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center (PIC) at (972) 644–5580. When ordering, please identify this booklet by its title and literature number. Updated documents can also be obtained through our website at www.ti.com.

Data Sheets:	**Literature Number:**
ADS7861	SBAS110
ADS8361	SBAS230
Op Amps for Everyone	SLOD006

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Trademarks

Contents

Tables

Chapter 1

EVM Overview

The ADS7861 and ADS8361 are high-speed, low-power, 12-bit and 16-bit A/D converters that operate from independent 5-V AV_{DD} and 5-V D_{VDD} (2.7-V to 3.6-V DV_{DD} for ADS8361) supplies.

The four fully differential analog inputs are divided into two pairs (A and B). The ADS7861 and ADS8361 accept an analog input voltage in the range of –VREF to +VREF (5 $V_{p–p}$), centered on the internal 2.5-V reference. The part also accepts bipolar input ranges when a level shift circuit is used in the analog front-end circuitry. Refer to Section 12 of *Op Amps for Everyone* (literature number SLOD006) for information on various circuit applications.

Topic **Page**

1.1 Features

- Full-featured evaluation board for the ADS7861 and ADS8361, dual, 500-kSPS, 12-bit/16-bit, serial output, 2+2 analog input, simultaneous sampling analog-to-digital converter
- Analog inputs can be configured as single-ended or differential
- Built-in reference
- High-speed serial interface

Chapter 2

Analog Interface

For maximum flexibility, the ADS7861/8361 EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW–110–22–F–D–VS–K and TSM–110–01–T–DV–P provide a convenient ten-pin dual row header/socket combination at J1. This header/socket provides access to the analog input pins of the ADC. Consult Samtec at www.samtec.com or call 1–800–SAMTEC–9 for a variety of mating connector options.

Table 2–1. Header/Socket J1 Description

Pin Number	Signal	Description
J1.2	B1+	Noninverting input – channel B1
J1.4	B1–	Inverting input – channel B1
J1.6	B0+	Noninverting input – channel B0
J1.8	B0–	Inverting input – channel B0
J1.10	A1+	Noninverting input – channel A1
J1.12	A1–	Inverting input – channel A1
J1.14	A0+	Noninverting input – channel A0
J1.16	A0–	Inverting input – channel A0
J1.18	Unused	Pins are unused and should be left open for use with future amplifier and sensor input modules.
J1.20	REFIN	External reference source input (2.5 V nom, 2.525 V max)
J1.1– J1.19 (odd)	AGND	Analog ground connections

Chapter 3

Digital Interface

The ADS7861/8361 EVM is designed for easy interfacing to multiple control platforms. Samtec part numbers SSW–110–22–F–D–VS–K and TSM–110–01–T–DV–P provide a convenient ten-pin dual row header/socket combination at J2. This header/socket provides access to the digital control and serial data pins of the ADS7861/8361. Consult Samtec at www.samtec.com or 1–800–SAMTEC–9 for a variety of mating connector options.

Table 3–1. Header/Socket J2 Description

Pin Number	Signal	Description
J2.1	$\overline{CS}$	Chip select—Active low signal, enables data transfer and device configuration
J2.3	SCLK	Serial clock
J2.5	SCLK(R)	Serial clock return for DSP host
J2.7	FS	Frame sync
J2.9	FS(R)	Frame sync return for DSP host
J2.11	SDI	Serial data input
J2.13	SDO	Serial data output
J2.15	$\overline{INT}$	Interrupt output—provides an interrupt source to the host processor
J2.17	$\overline{CSTART}$	Conversion start—provides an alternate method of conversion initialization
J2.19	SPARE	

Topic **Page**

3.1 Additional Control Options

The following table shows the pin-out of header J5. This dual row, four-position header provides additional control functionality to the ADS7861/8361 EVM. Signals A0, M0, and M1 are configured with pull-up resistors by default. The jumper shunts supplied with the EVM can be used to set these signals to logic low. These signals can also be connected to control signals in the users system.

Table 3–2. Header J5 Description

Pin Number	Signal	Description
J5.1	M0	Selects two-channel or four-channel mode
J5.3	M1	Selects between serial outputs A and B
J5.5	A0	Operates in conjunction with M0. See data sheet for details.
J5.7	OUT B	B channel secondary output
J5.2 – J5.8 (even)	DGND	Digital ground connections

Chapter 4

Power Supplies

The ADS7861 EVM board requires 5 V dc for both the analog and digital sections of the ADC. While filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source. Positive 5-V dc power is applied to J3 and J4 (pin1 referenced to pin 2). The ADS8361 requires 5 V dc for the analog supply located on J3, and 2.7 V to 5.5 V dc for the digital supply located on J4.

An alternate power source can be applied via J6 located on the bottom side of the printed-circuit board. If a variable digital supply voltage is desired, completely remove the shunt jumper from W3. Apply a 100-mA current limited dc voltage of not more than 5.5 V to J4.

Note:

The shunt jumper at location W3 should be placed across pin 2 and pin 3 for proper operation of the ADS7861. This is the factory default condition for both the ADS7861 and ADS8361 EVMs.

Topic **Page**

4.1 Reference Voltage

The ADS7861/8361 can be configured to use its internal reference, or external reference source through jumper W1 (see schematic for details). If an external reference is desired, the shunt jumper on W1 should cover pins 2 and 3. The external reference is supplied through header/socket J1 pin 20 (J1.20).

Chapter 5

EVM Operation

Apply a current limited (150 mA max) 5-V dc source to J3 and J4 prior to connecting the analog input signals and digital control signals.

The analog input source can be applied directly to header/socket J1 (top or bottom side) or through optional amplifier and signal conditioning modules. The analog input level should not exceed 5 $V_{p–p}$.The analog input range is from –VREF to VREF (0 V to 5 Vdc) centered at 2.5 V.

The digital control signals can be applied directly to header/socket J2 (top or bottom side). The ADS7861/8361 EVM can also be connected directly to a DSP interface board. Consult the ADS7861 and ADS8361 product folders for a complete list of DSP interface cards and optional analog interface modules.

Jumper W2 is provided to allow separation of the convert start (CONVST) and read (RD) signals. The factory default condition for the EVM is to place a shunt jumper between pin 1 and pin 2 of W2. This combines signals RD and CONVST, which are applied to the ADC via pin J2.7. When W2 is moved to pin 2 and pin 3, the RD signal is applied via pin J2.7 while CONVST is applied to pin J2.17.

Header J5 is a means to access the M0, M1, and A1 control lines as well as the OUTB serial data. Shunt jumpers are placed on pins 1 and 2, 3 and 4, and 5 and 6 of J5, which defaults M0, M1, and A0 to logic low levels. Removing the jumpers allows these lines to go to logic high levels through the associated pullup resistors R12, R13, and R14. In the factory default conditions, the ADC is converting the A0 and B0 inputs, placing AOUT serial data on pin J2.13, and BOUT serial data on pin J5.7.

Chapter 6

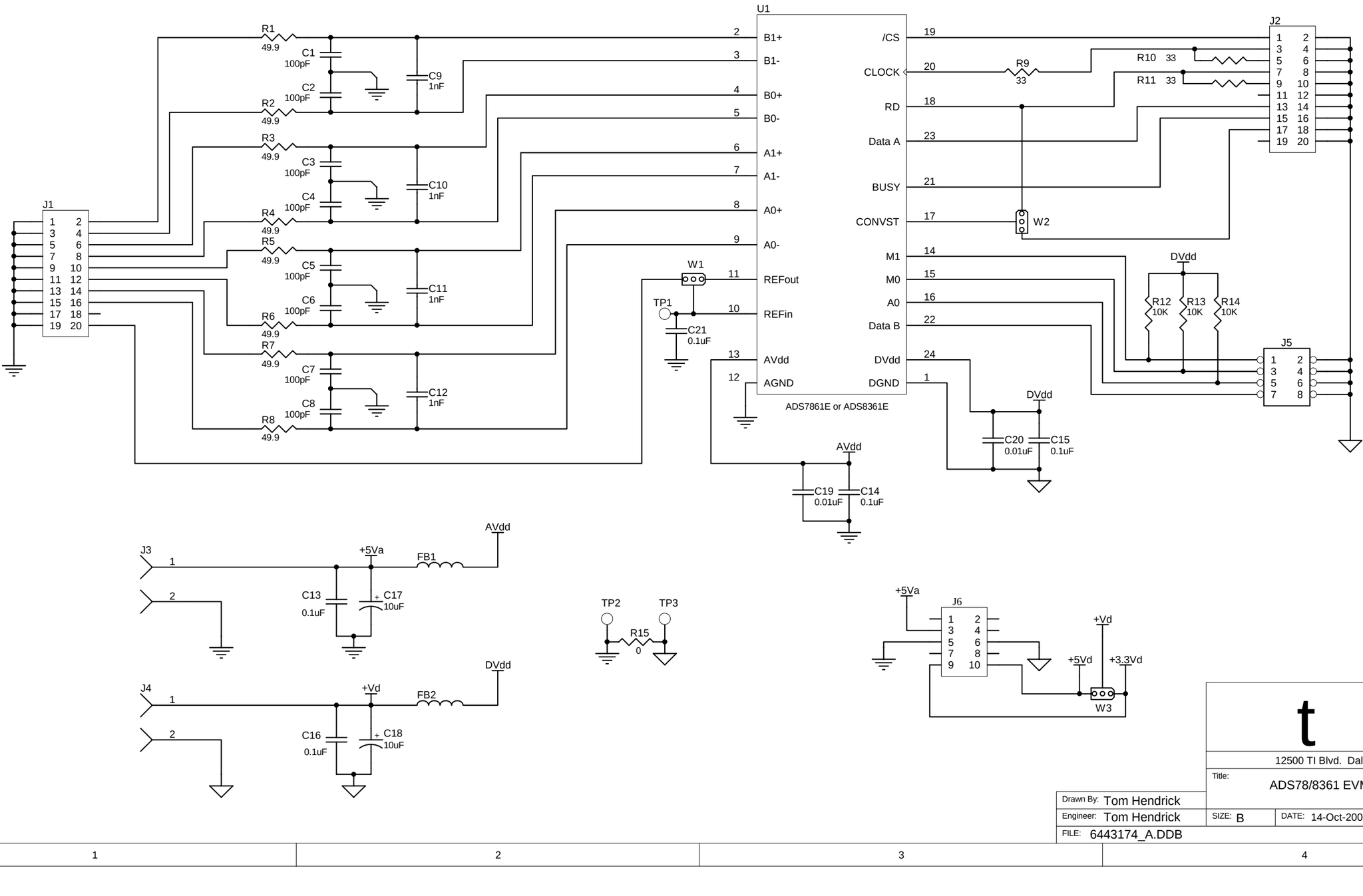
Bill of Materials and EVM Schematic

The following table contains a complete bill of materials for the ADS7861/8361 EVM. The schematic diagram is also provided for reference.

Table 6–1. Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
C1 C2 C3 C4 C5 C6 C7 C8	100-pF, 0805, Ceramic capacitor, NPO, 50-V, 5%	PhyComp	0805CG101J9B200
C13 C14 C15 C16 C21	0.1-μF, 0805, Ceramic capacitor, X7R, 50-V, 10%	Panasonic	ECJ–2YB1H104K
C17 C18	10-μF, 16-V, Aluminum capacitor, Size C	Cornell Dubilier	AVS106M16B12T
FB1 FB2	SMT, EMI beads, Z = 47 Ω at 100 MHz	Fair-Rite	2743019447
J1 J2 (top side)	10 Pin, dual row, SMT header (20 Position)	Samtec	TSM–110–01–T–DV–P
J1B J2B (bottom side)	10 Pin, dual row, SMT socket (20 Position)	Samtec	SSW–110–22–F–D–VS–K
J3 J4	2 Terminal screw connector	OST	ED1514
J5	4 Pin, dual row, TH header (8 Position)	Samtec	TSW–104–07–L–D
J6 (bottom side)	4 Pin, dual row, TH header (8 Position)	Samtec	SSW–105–22–F–D–VS–K
R1 R2 R3 R4 R5 R6 R7 R8	49.9-Ω, 0805, 1%, 0.1-W resistor	Yageo America	9C08052A49R9FKHFT
R9 R10 R11	33-Ω, 0805, 5%, 0.1-W resistor	Yageo America	9C08052A33R0JLHFT
R12 R13 R14	10-kΩ, 0805, 0.1-W resistor	Yageo America	9C08052A1002JLHFT
R15	0-Ω, 0805, 0.1-W resistor	Yageo America	9C08052A0R00JLHFT
TP1 TP2 TP3	Red test point loop	Keystone	5000
U1	ADS7861 or ADS8361 ADC	Texas Instruments	ADS7861E or ADS8361I
W1	3 Pin, 2-mm header	Samtec	TMM–103–01–G–S
W2, W3	3 Pin header	Samtec	TSW–103–07–L–S

Revision History		
REV	ECN Number	Approved



Drawn By: Tom Hendrick			
Engineer: Tom Hendrick	SIZE: B	DATE: 14-Oct-2002	REV: A
FILE: 6443174_A.DDB			SHEET: 1 OF: 1

12500 TI Blvd. Dallas, Texas 75243

Title: ADS78/8361 EVM Schematic